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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,918	09/22/2003	Masanori Ogura	03500.017569.	5148

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EXAMINER

KHAN, USMAN A

ART UNIT	PAPER NUMBER
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2622

MAIL DATE	DELIVERY MODE
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08/07/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<p align="center">Office Action Summary</p>	<p>Application No.</p> <p align="center">10/664,918</p>	<p>Applicant(s)</p> <p align="center">OGURA ET AL.</p>	
	<p>Examiner</p> <p align="center">Usman Khan</p>	<p>Art Unit</p> <p align="center">2622</p>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 and 08 March 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/25/2007 has been entered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 2, 5 – 10, and 14 - 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Umeda et al. (US patent No. 6,452,632).

Regarding **claim 1**, Umeda et al. teaches a solid state image pick-up device formed on a chip (column 1 lines 9 *et seq.* and column 9 lines 7 *et seq.* also figure 72), comprising: a pixel region (figure 72; item 502); a first shift register for reading a signal

charge from the pixel region (figure 72; item 512); a second shift register having a lower driving frequency than that of the first shift register (figure 72; item 511, also it is inherent that horizontal shift registers have a higher driving frequency than vertical shift registers), wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 72; items 511 and 512); an amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 72, item 504), outputting video signals (figure 72, outputting analog signal following item 504); and a pad for outputting the video signals to an outside of the chip (figure 72, outputting analog signal following item 504 through pad shown as a small circle in the figure), the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged (figure 72 pad following item 504).

Regarding **claim 2**, as mentioned above in the discussion of claim 1, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that in the pixel region, pixels having an active element are two-dimensionally arranged (figure 72 item 502).

Regarding **claim 5**, as mentioned above in the discussion of claim 2, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that the pixel region is formed into a rectangle, and the first shift register is arranged closer to a long side of the pixel region (figure 72; items 502, 511, and 512).

Regarding **claim 6**, as mentioned above in the discussion of claim 5, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that the pixel region is sandwiched by shift registers (figure 72, shift register 511 and 512 in essence sandwich the region of item 502 close to where they form a right angle to each other).

Regarding **claim 7**, as mentioned above in the discussion of claim 2, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that the first shift register is a horizontal shift register (figure 72; item 512), and the second shift register is a vertical shift register (figure 72; item 511).

Regarding **claim 8**, Umeda et al. teaches a camera, comprising: the solid state image pick-up device according to claim 1 (see discussion of claim 1); a lens for forming an optical image of a subject (figures 15, 16, 18, 24, 26, 37, 39, items 302 and 100); and a signal processing unit for processing a signal from the solid state image pick-up device (figure 72, item 507).

Regarding **claim 9**, Umeda et al. teaches a solid state image pick-up device formed on a chip (column 1 lines 9 *et seq.* and column 9 lines 7 *et seq.* also figure 72), comprising: a pixel region (figure 72; item 502); a first shift register for reading a signal charge from the pixel region (figure 72; item 512); a second shift register having lower

driving frequency than that of the first shift register (figure 72; item 511, also it is inherent that horizontal shift registers have a higher driving frequency than vertical shift registers), wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 72; items 511 and 512); an amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 72, item 504), outputting video signals (figure 72, outputting analog signal following item 504); and a pad for supplying a voltage to the amplifier (it is inherent that amplifier 504 is run by a supplied voltage through a pad), the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged (figure 72 pad following item 504).

Regarding **claim 10**, Umeda et al. teaches a solid state image pick-up device formed on a chip (column 1 lines 9 *et seq.* and column 9 lines 7 *et seq.* also figure 72), comprising: a pixel region (figure 72; item 502); a first shift register for reading a signal charge from the pixel region (figure 72; item 512); a second shift register having a lower driving frequency than that of the first shift register (figure 72; item 511, also it is inherent that horizontal shift registers have a higher driving frequency than vertical shift registers), wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 72; items 511 and 512); an amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 72, item 504), outputting video signals (figure 72, outputting analog signal following item 504); and a pad for supplying a predetermined voltage or a ground voltage to an active

Art Unit: 2622

element included in a pixel in the pixel region (it is inherent that the imager is run by a supplied voltage through a pad; also, column 1 lines 33 – 47), the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged (figure 72 pad following item 504).

Regarding **claim 14**, as mentioned above in the discussion of claim 1, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that the pad is arranged only along a side portion of the chip at an angle of 90 degrees to the side portion along which the first shift register is arranged (figure 72 pad following item 504).

Regarding **claim 15**, as mentioned above in the discussion of claim 9, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that the pad is arranged only along a side portion of the chip at an angle of 90 degrees to the side portion along which the first shift register is arranged (figure 72 pad following item 504).

Regarding **claim 16**, as mentioned above in the discussion of claim 10, Umeda et al. teaches all of the limitations of the parent claim. Additionally, Umeda et al. teaches that the pad is arranged only along a side portion of the chip at an angle of 90 degrees to the side portion along which the first shift register is arranged (figure 72 pad following item 504).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Umeda et al. (US patent No. 6,452,632) in further view of Itano et al. (US PgPub 2002/0051071).

Regarding **claim 3**, as mentioned above in the discussion of claim 2, Umeda et al. teaches all of the limitations of the parent claim. However, Umeda et al. fails to disclose that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor. Itano et al., on the other hand teaches that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor.

More specifically, Itano et al. teaches the active element comprises at least one selected from the group consisting of a transfer MOS transistor (figure 1 item 105, and paragraph 0006), a reset MOS transistor (figure 1 items 110a and 110b, and paragraph 0006), a source follower input MOS transistor (figure 1 item 107, and paragraphs 0006, 0048, 0051), and a selection MOS transistor (paragraph 0051).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Itano et al. with the teachings of Umeda et al. for reduction of size and in turn cost as taught in paragraph 0021 of Itano et al.

Claims 11 - 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Umeda et al. (US patent No. 6,452,632) in further view of Applicants Admitted Prior Art.

Regarding **claim 11**, as mentioned above in the discussion of claim 1 Umeda et al. teaches all of the limitations of the parent claims.

However, Umeda et al. fails to disclose that the side portions along which the first and second shift registers are arranged are adjacent to each other. Applicants Admitted Prior Art, on the other hand teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other.

More specifically, Applicants Admitted Prior Art teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine applicants admitted prior art of horizontal and vertical shift registers with the teachings of Umeda et al. to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up

element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Regarding **claim 12**, as mentioned above in the discussion of claim 9 Umeda et al. teaches all of the limitations of the parent claims.

However, Umeda et al. fails to disclose that the side portions along which the first and second shift registers are arranged are adjacent to each other. Applicants Admitted Prior Art, on the other hand teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other.

More specifically, Applicants Admitted Prior Art teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine applicants admitted prior art of horizontal and vertical shift registers with the teachings of Umeda et al. to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Regarding **claim 13**, as mentioned above in the discussion of claim 10 Umeda et al. teaches all of the limitations of the parent claims.

However, Umeda et al. fails to disclose that the side portions along which the first and second shift registers are arranged are adjacent to each other. Applicants Admitted Prior Art, on the other hand teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other.

More specifically, Applicants Admitted Prior Art teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine applicants admitted prior art of horizontal and vertical shift registers with the teachings of Umeda et al. to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yonemoto et al. (US patent No. 6,166,769) teaches pads near the vertical shift registers.

Tanaka et al. (US patent No. 6,037,577) teaches pads near the vertical shift registers.

Shinohara (US patent No. 5,587,738) teaches pads near the vertical shift registers.

Kozuka et al. (US patent No. 6,118,115) teaches pads near the vertical shift registers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Usman Khan whose telephone number is (571) 270-1131. The examiner can normally be reached on Mon-Thru 6:45-4:15; Fri 6:45-3:15 or Alt. Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Usman Khan
08/01/2007
Patent Examiner
Art Unit 2622



DAVID OMETZ
SUPERVISORY PATENT EXAMINER